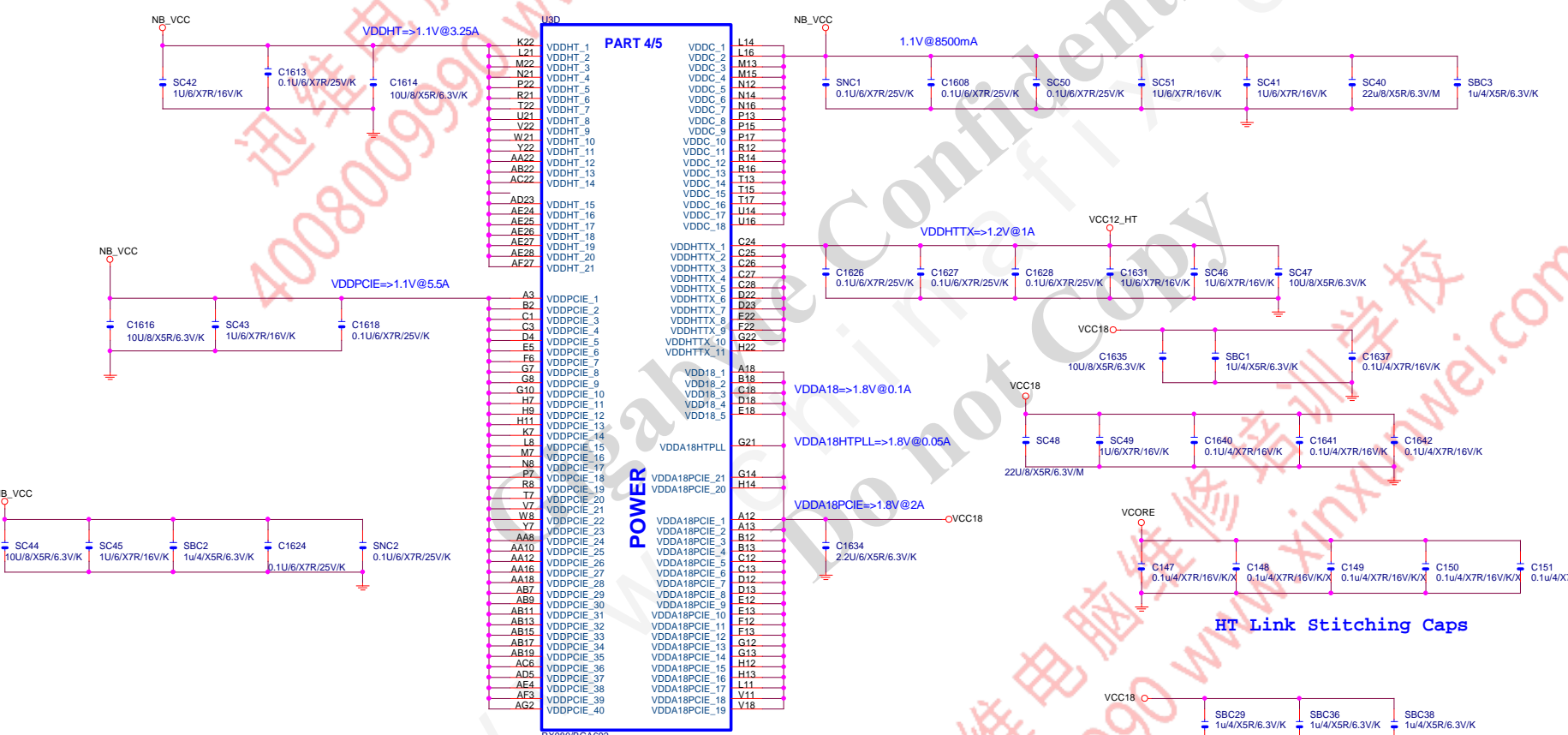


PART 5/5

GROUND

VS141 VS142 VS143 VS144 VS145 VS146 VS147 VS148 VS149 VS150 VS151 VS152 VS153 VS154 VS155 VS156 VS157 VS158 VS159 VS160 VS161 VS162 VS163 VS164 VS165 VS166 VS167 VS168 VS169 VS170 VS171 VS172 VS173 VS174 VS175 VS176 VS177 VS178 VS179 VS180 VS181 VS182 VS183 VS184 VS185 VS186 VS187 VS188 VS189 VS190 VS191 VS192 VS193 VS194 VS195 VS196 VS197 VS198 VS199 VS200 VS201 VS202 VS203 VS204 VS205 VS206 VS207 VS208 VS209 VS210 VS211 VS212 VS213 VS214 VS215 VS216 VS217 VS218 VS219 VS220 VS221 VS222 VS223 VS224 VS225 VS226 VS227 VS228 VS229 VS230 VS231 VS232 VS233 VS234 VS235 VS236 VS237 VS238 VS239 VS240 VS241 VS242 VS243 VS244 VS245 VS246 VS247 VS248 VS249 VS250 VS251 VS252 VS253 VS254 VS255 VS256 VS257 VS258 VS259 VS260 VS261



NB CLOCK INPUT TABLE

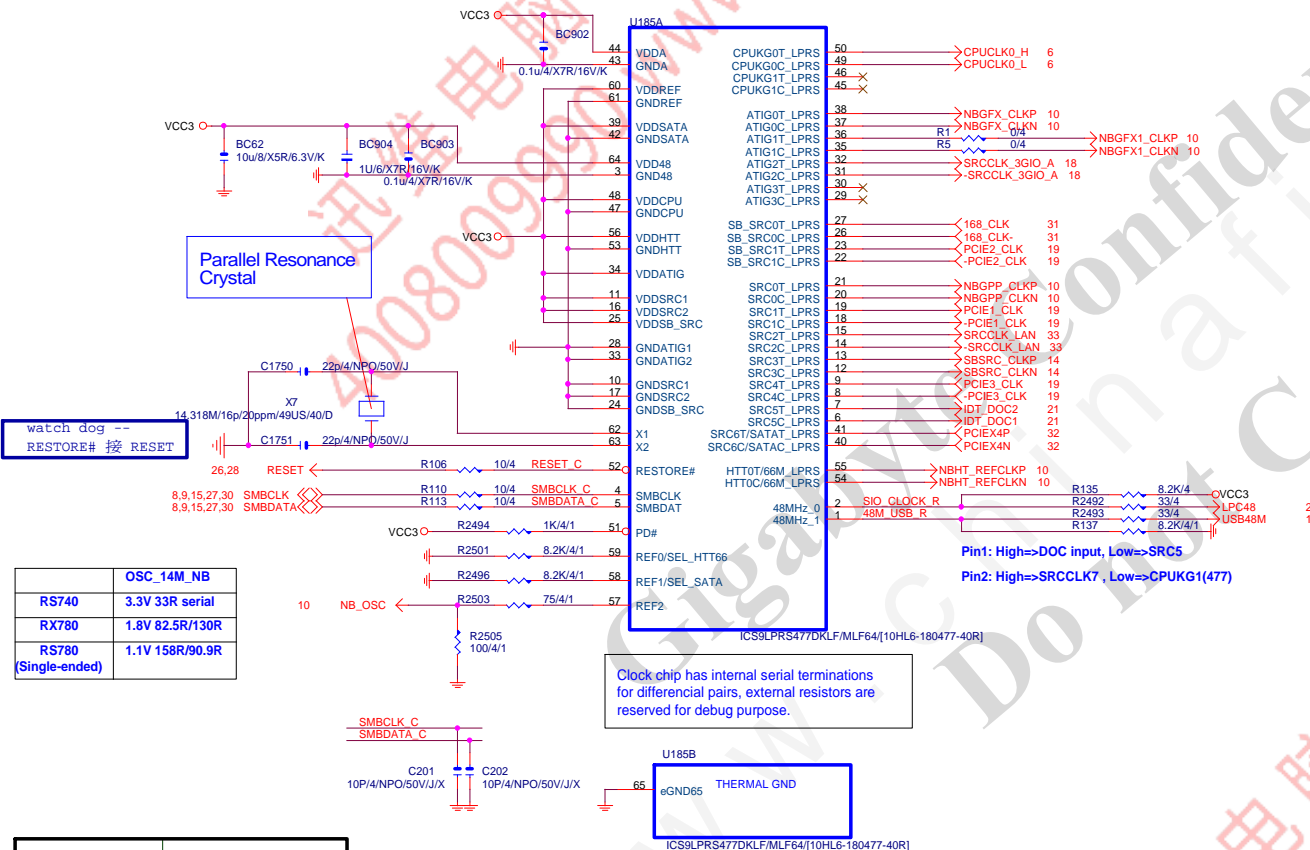
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

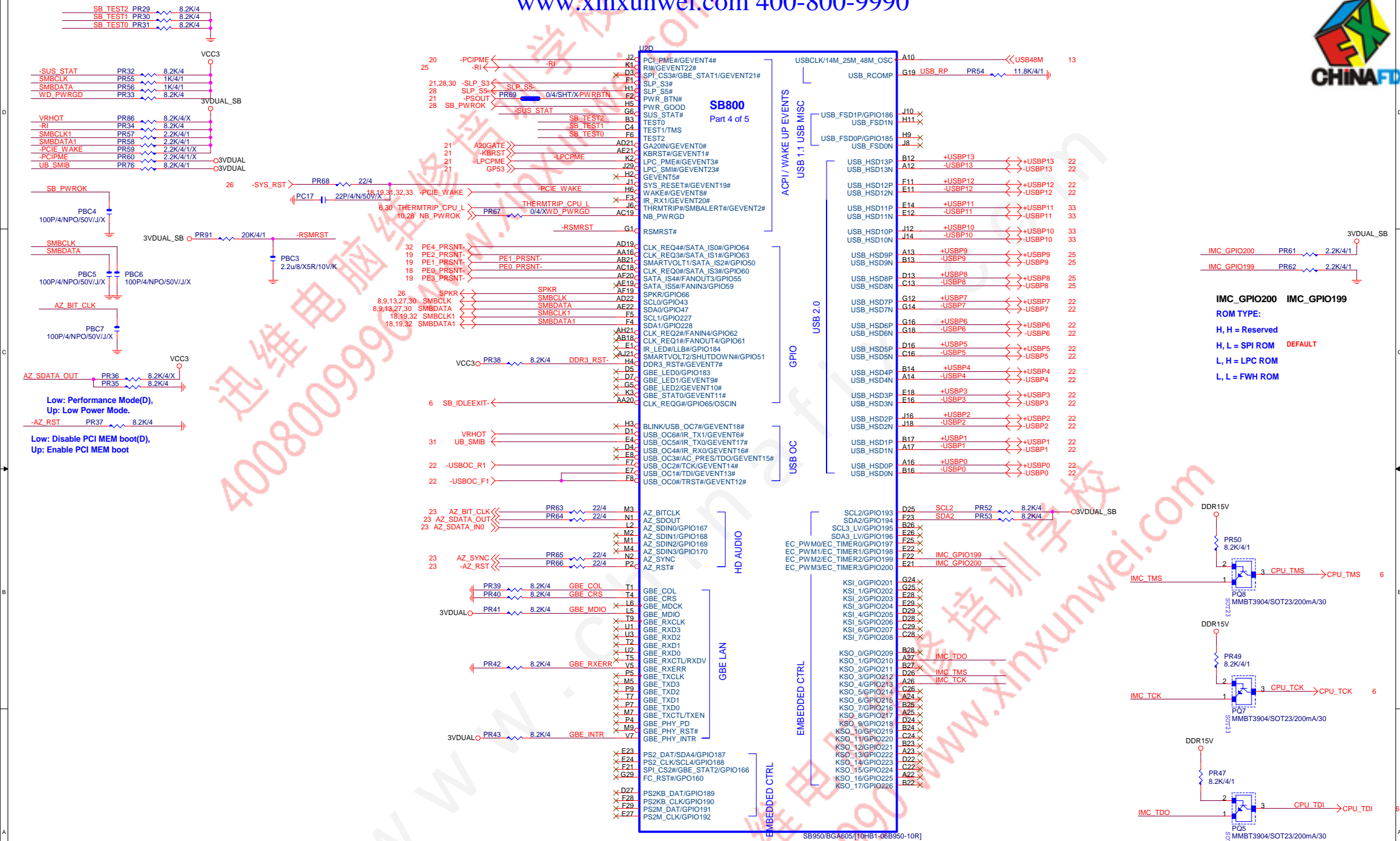


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Title RTM880N-793

Size Custom Document Number GA-970A-D3 Rev 1.41

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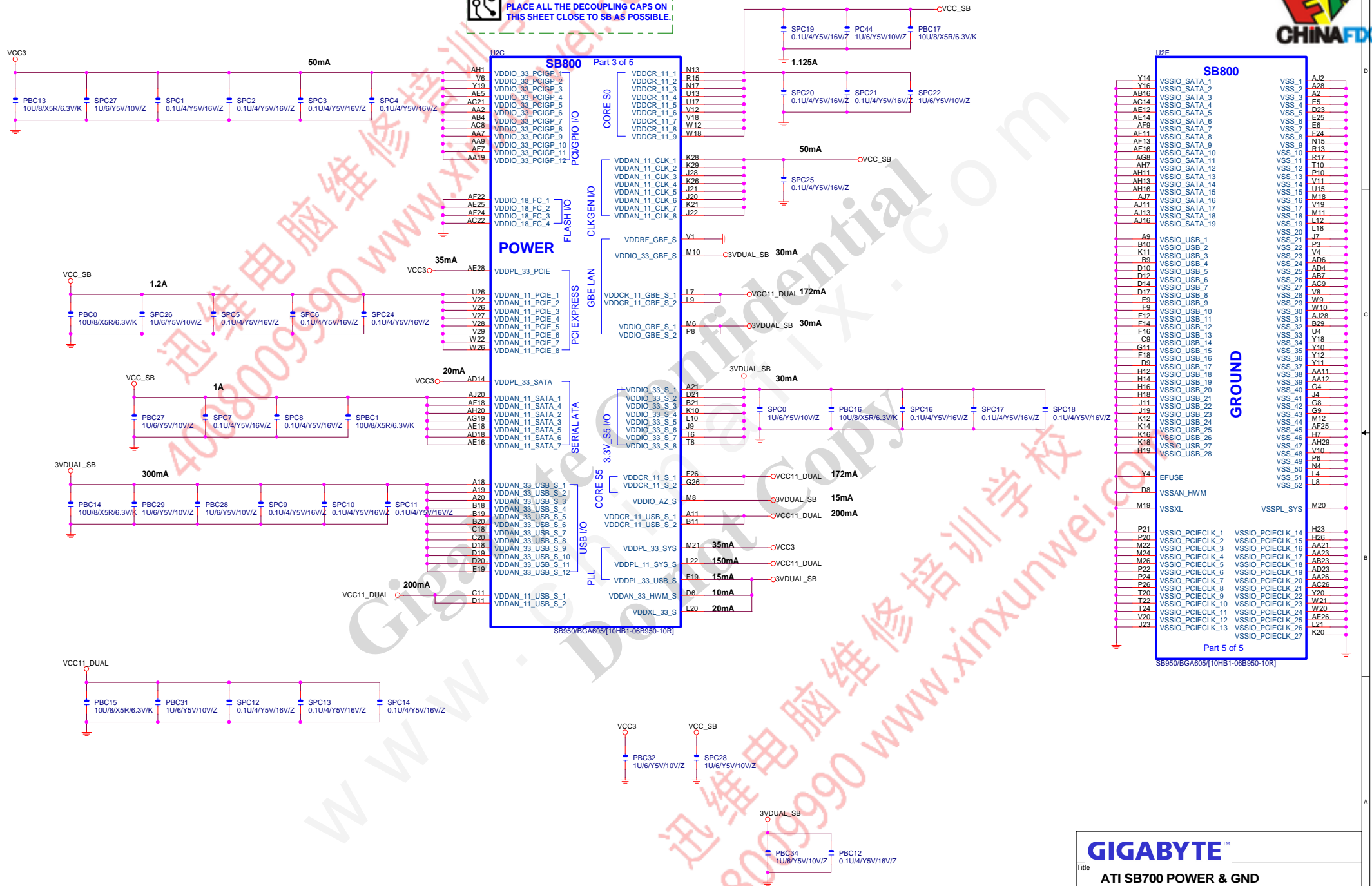

GIGABYTE™
ATI SB700 ACPI/USB/GPIO/AUDIO

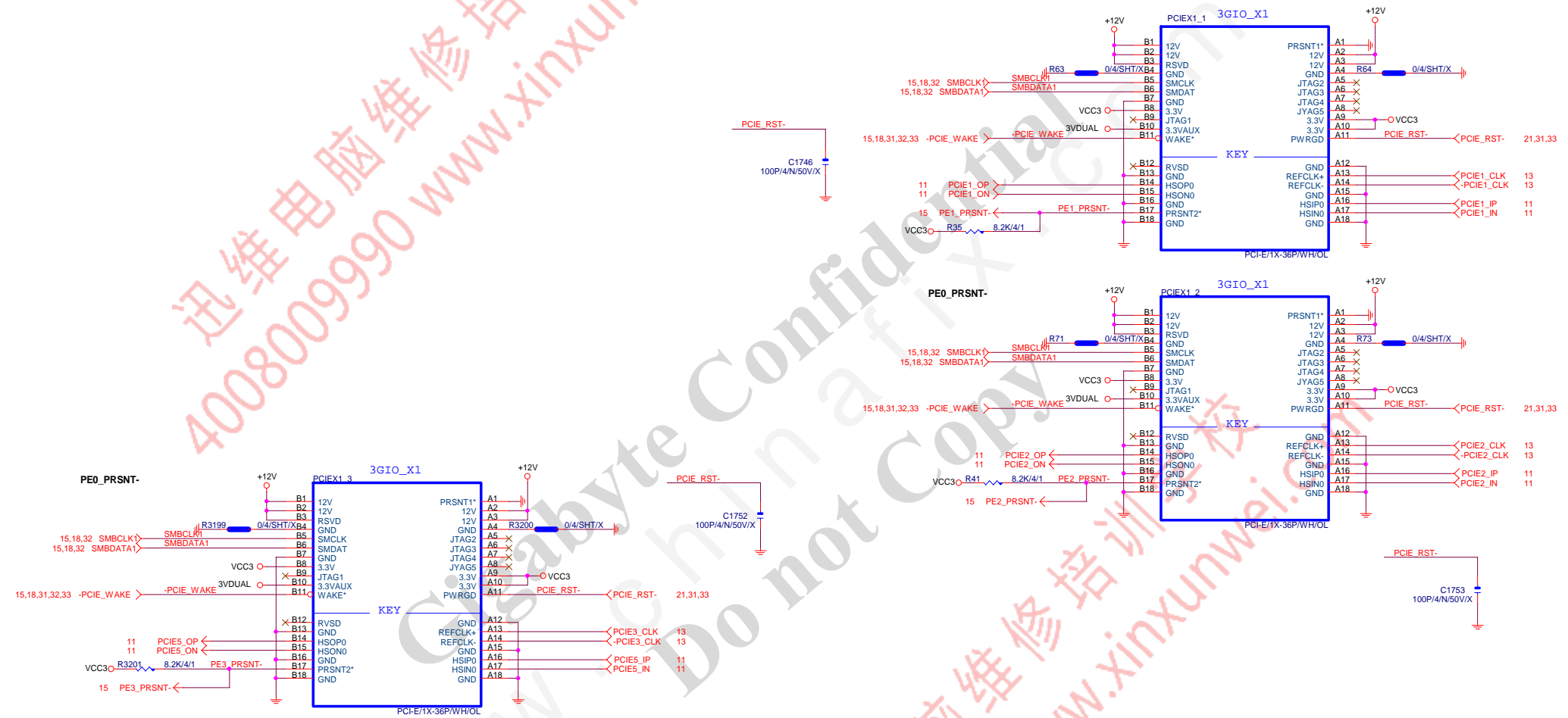
Size: Custom
 Document Number: **GA-970A-D3**
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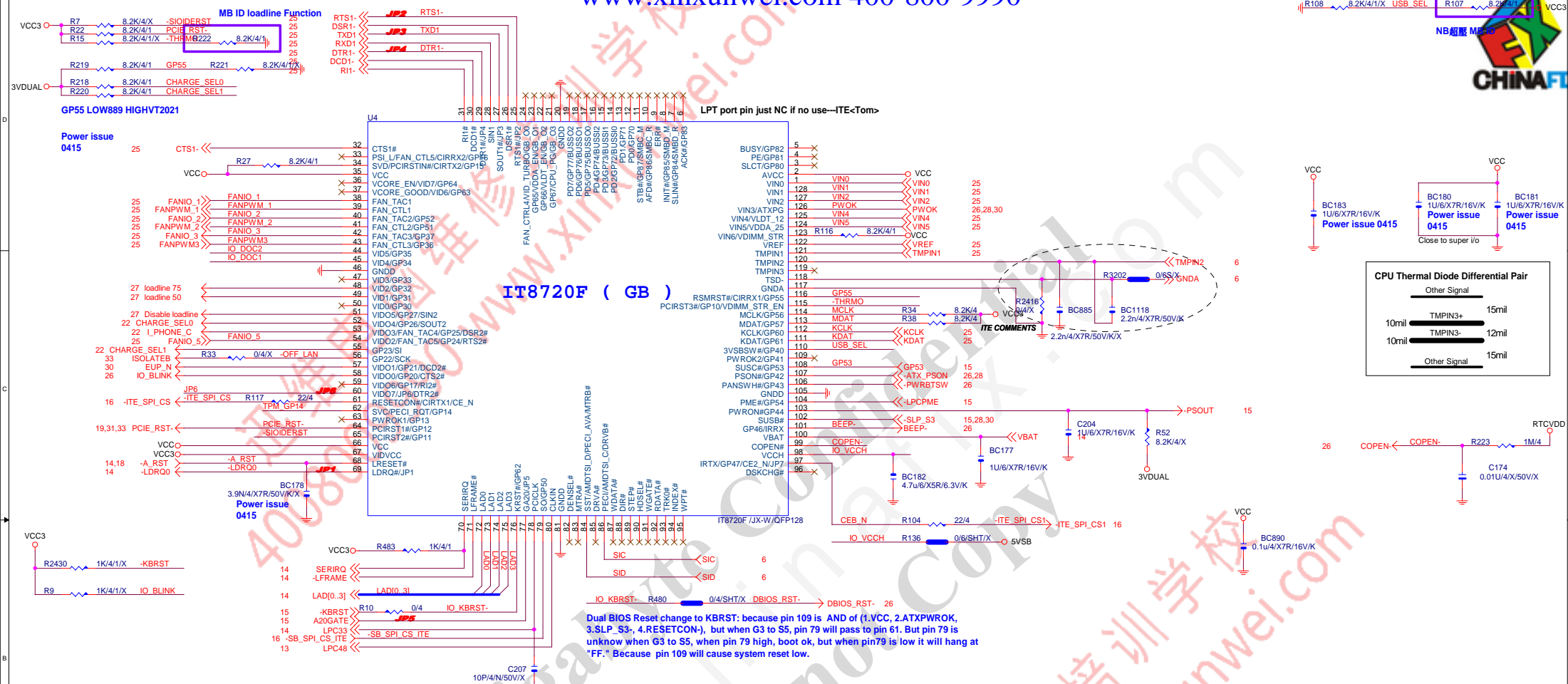
 Rev
1.41



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

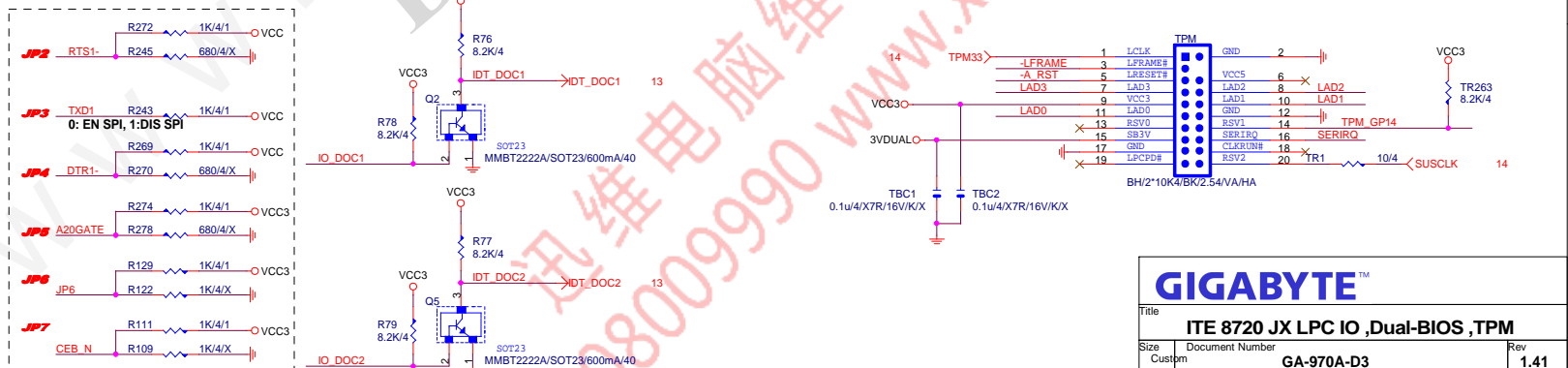




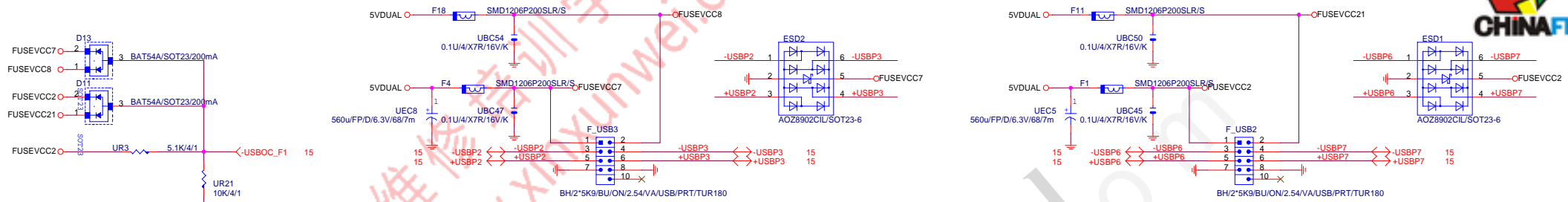


IT8720GB Power On Strapping Options

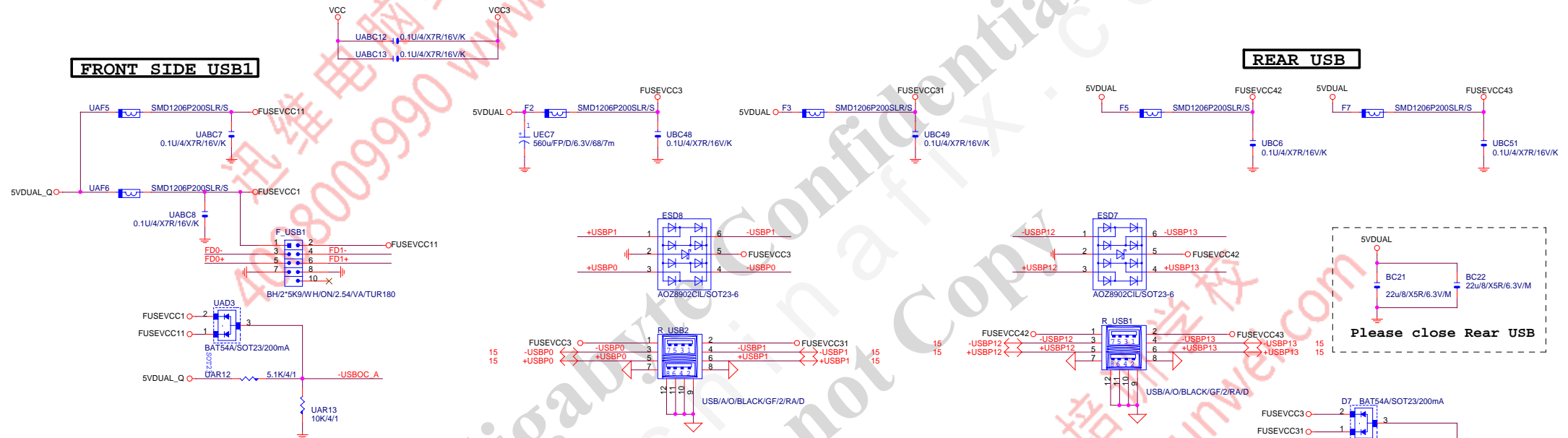
Symbol	value	Description
JP1		
Pin 69		
JP2	1	Disable VID output pins
Pin 25	0	Enable VID output pins
JP3	1	Disabled.
Pin 27	0	Flash I/F Address Segment 1 is enabled
JP4	1	K8 power sequence disabled
Pin 29	0	K8 power sequence enabled
JP3 & JP5	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	10 No Run	Default value of EC Index 15h/16h/17h is 7fh
	01 Full Run	Default value of EC Index 15h/16h/17h is 00h
	00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5	1	Disable WDT to rest PWROK
Pin 77	0	Enable WDT to rest PWROK
JP6	1	Disable SVID Function
Pin 60	0	Enable SVID Function
JP7	1	Enable Dual BIOS Function for GigaByte Only
Pin 97	0	Disable Dual BIOS Function for GigaByte Only



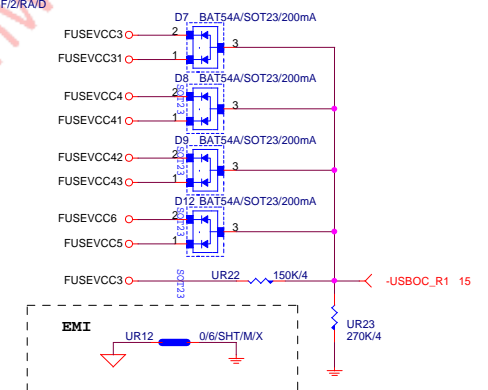
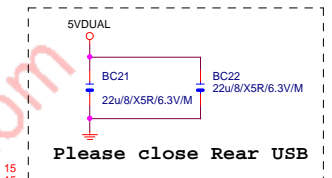
FRONT SIDE USB2



FRONT SIDE USB1



REAR USB

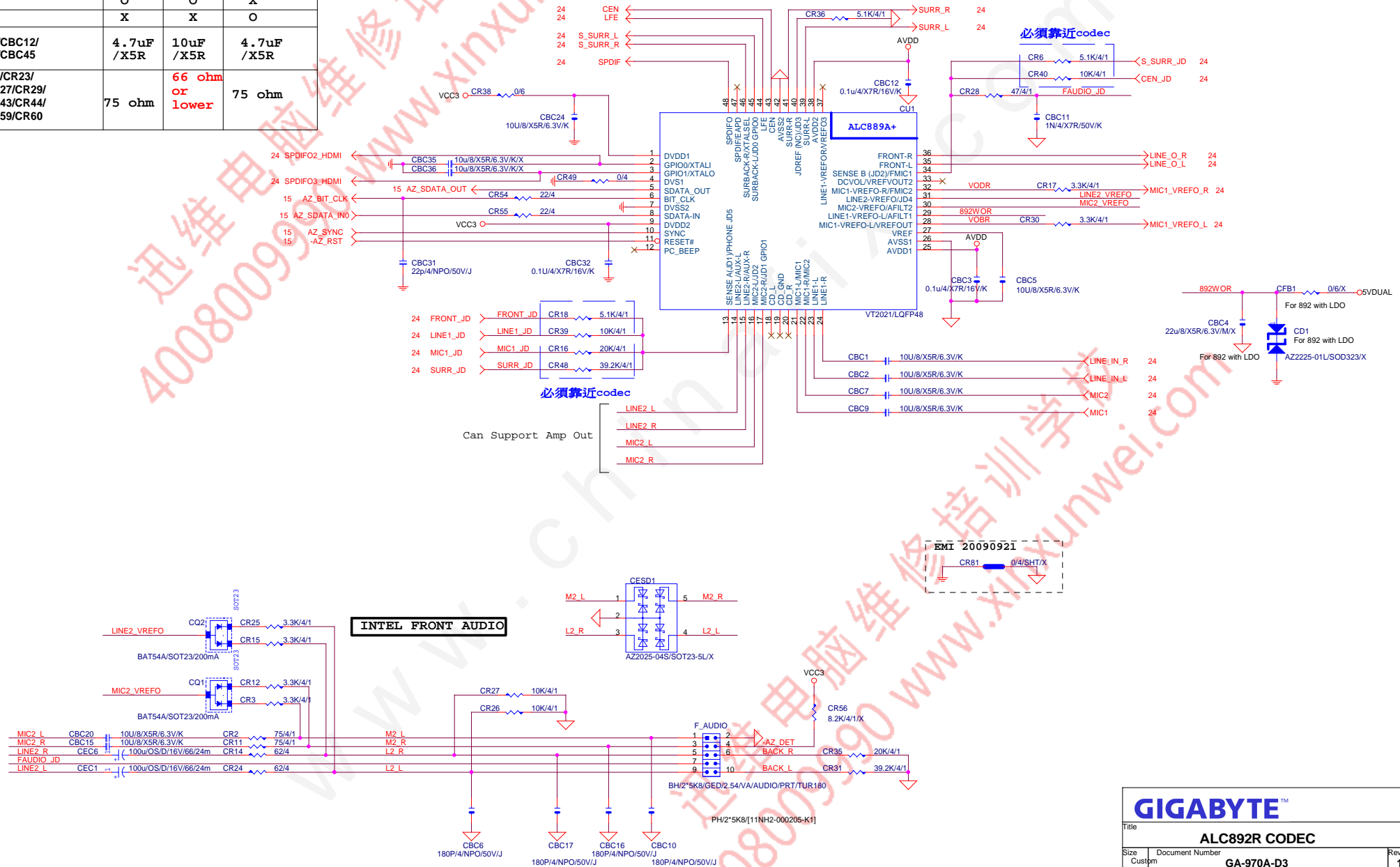


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COM/LPT/F_USB/PWR

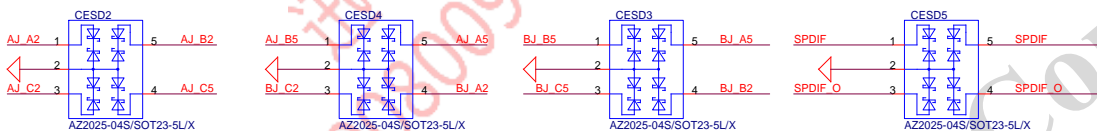
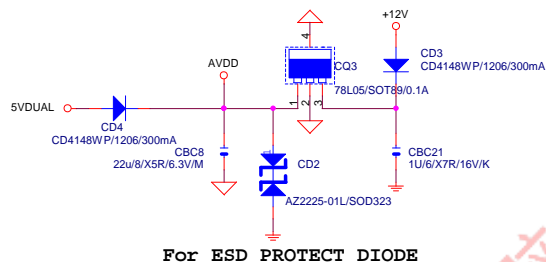
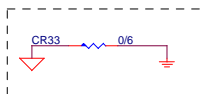
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	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

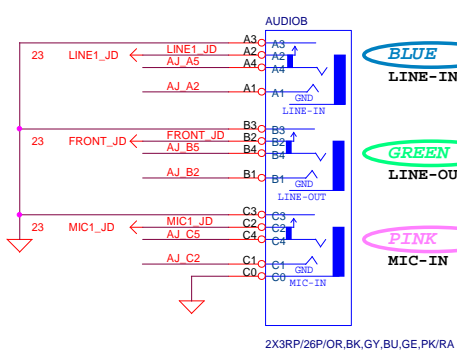


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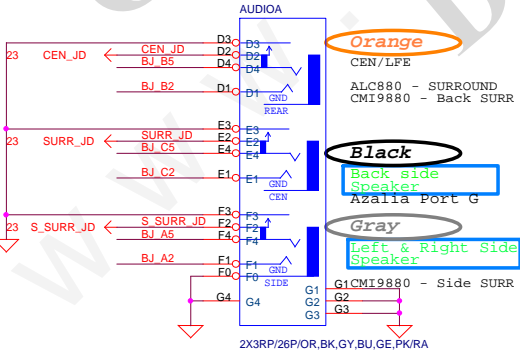
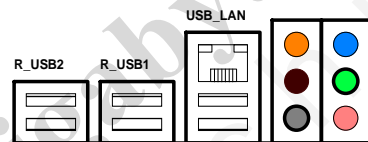
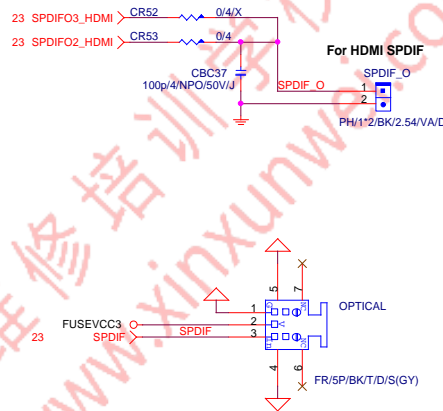


For Audio precision test



A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15P/[11NR6-403004-11]

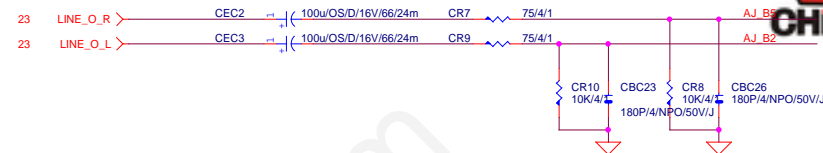
SPDIF



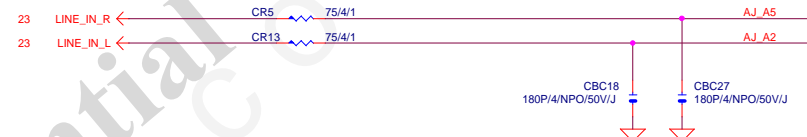
A3RJ/13P/0BG/[11NR6-403006-71]
3RJ+15P/[11NR6-403004-31]

www.xinxunwei.com 400-800-9990

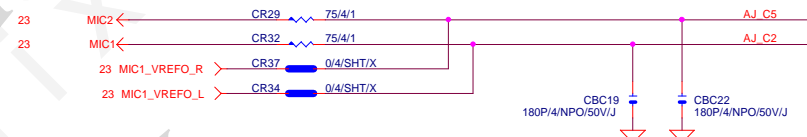
LINE OUT
FRONT OUT



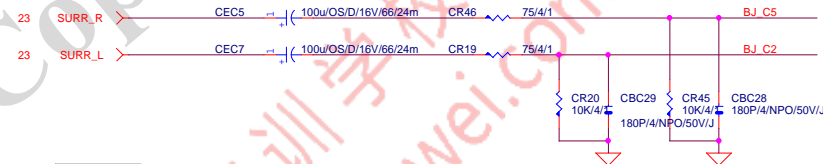
LINE-IN



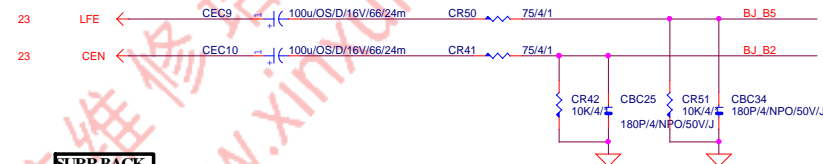
MIC



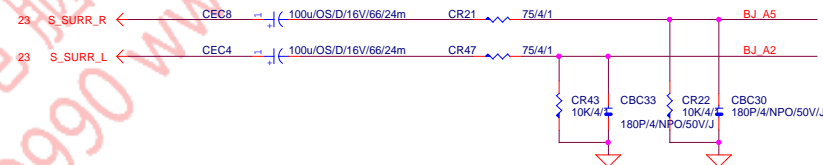
SURROUND



CEN/LFE



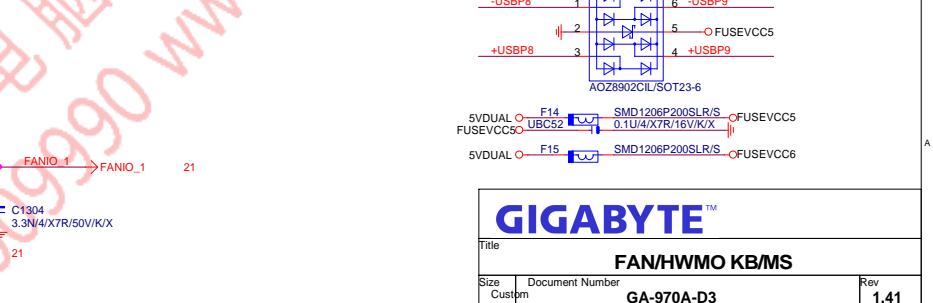
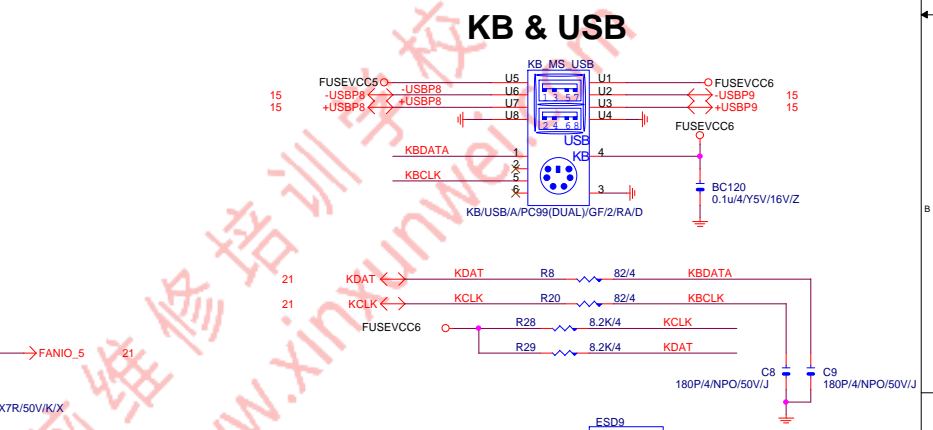
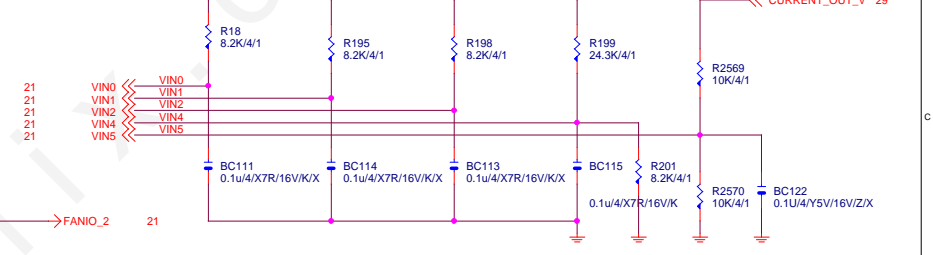
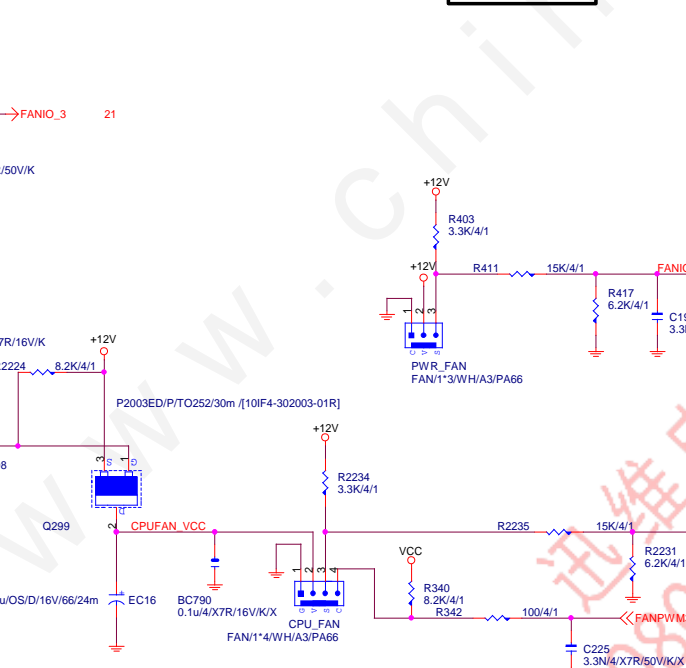
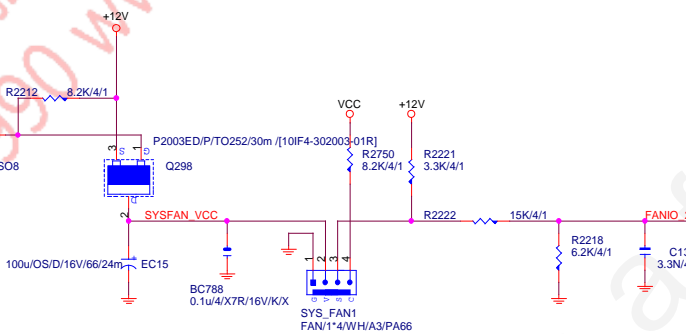
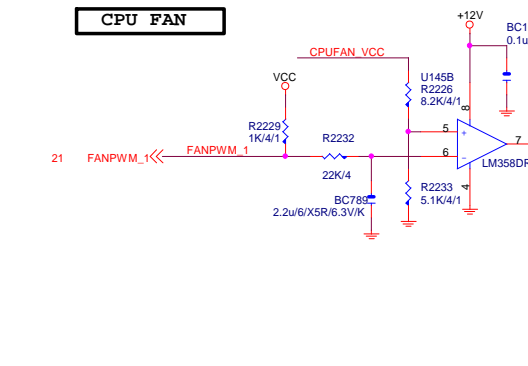
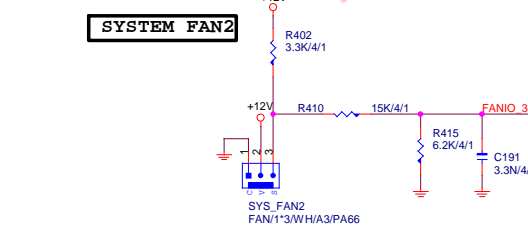
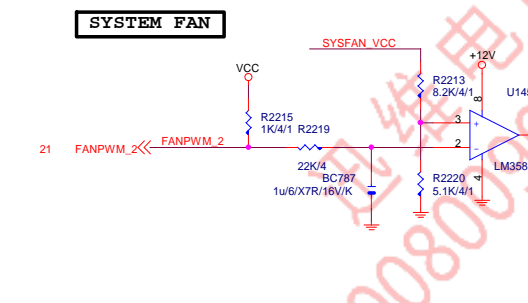
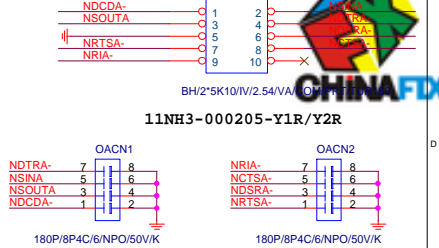
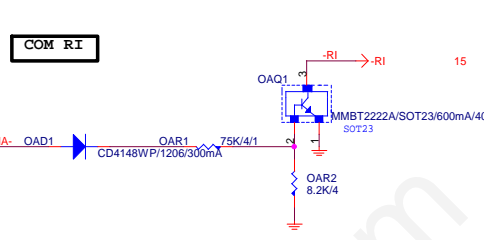
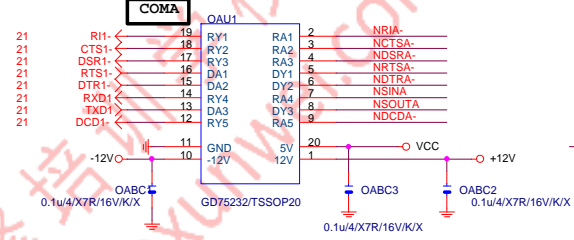
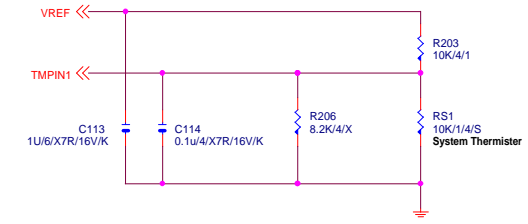
SURRBACK

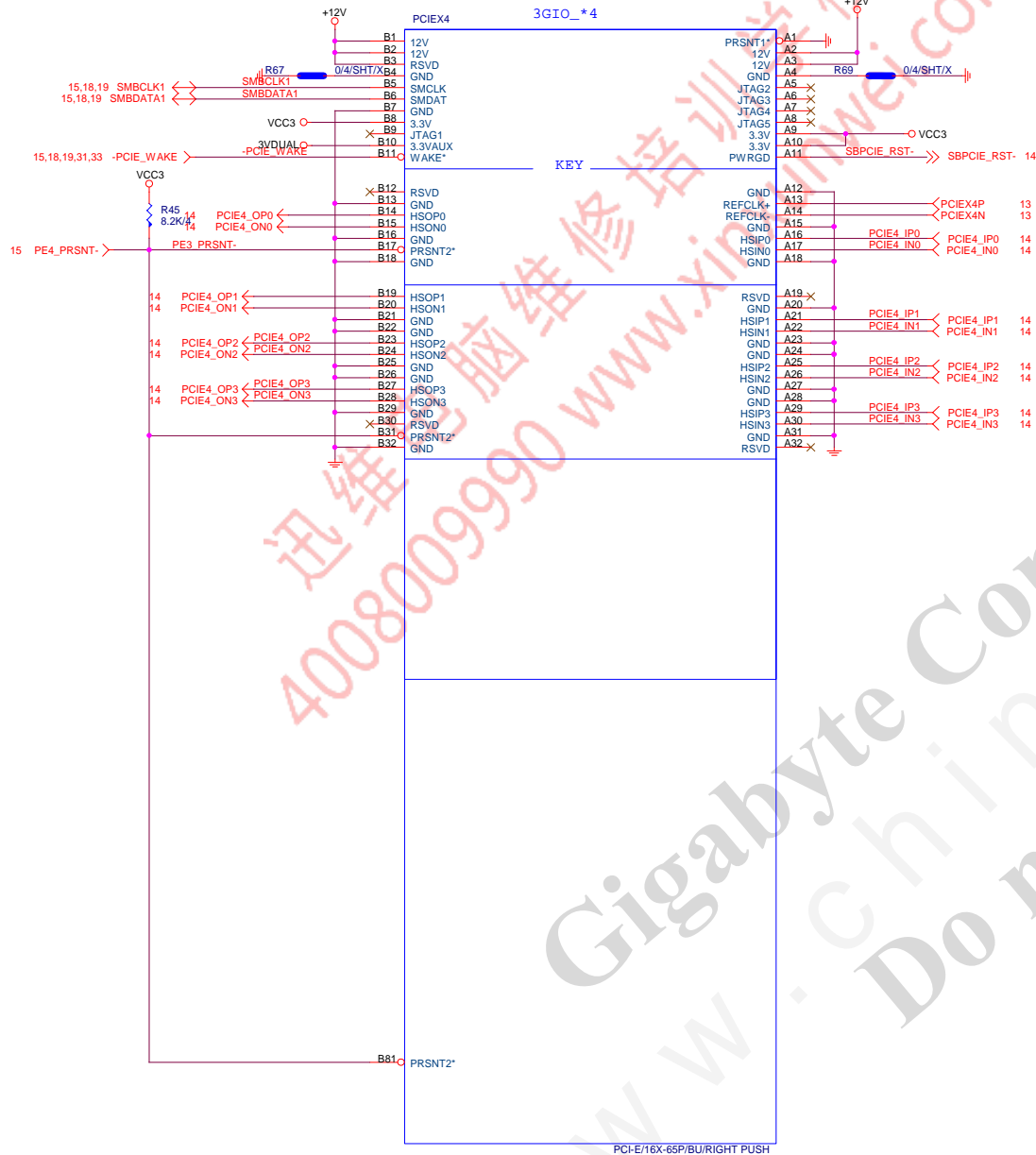


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Hardware Monitor circuits



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